Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A host controller, for use in a bus communication device comprising a host microprocessor and a system memory, the host controller comprising:

a first interface for connection to a memory bus which connects the host microprocessor and the system memory, such that the host controller is adapted to act only as a slave on the memory bus;

an internal memory, for storing a plurality of transfer-based transfer descriptors received through the first interface; and

a second interface, for connection to an external bus,

wherein the host controller is adapted to:

execute stored transfer-based transfer descriptors;

update the content of the stored transfer-based transfer descriptors on execution; and

copy the updated stored transfer-based transfer descriptors to the system memory.

2. (original) A host controller as claimed in claim 1, wherein the internal memory is a dual-port RAM.

3. (original) A host controller as claimed in claim 1, wherein the internal memory is a single-port RAM, and the host controller further comprises an arbiter to allow data to be written to and read from the RAM essentially simultaneously.

4. (original) A host controller as claimed in claim 1, wherein the internal memory is divided into two parts, and is adapted to store transfer-based transfer descriptor headers in a first part, and to store transfer-based transfer descriptor payload data in a second part.

5. (original) A host controller as claimed in claim 4, wherein the first part of the internal memory is sub-divided into two sub-parts, and is adapted to store transfer descriptor headers relating to periodic transfers in a first subpart, and to store transfer descriptor headers relating to asynchronous transfers in a second sub-part.

6. (original) A host controller as claimed in claim 5, wherein the host controller is adapted to scan the first sub-part of the internal memory once in each micro-frame, and is adapted to scan the second sub-part continuously throughout each micro-frame.

7. (original) A host controller as claimed in claim 1, wherein the host controller is a USB host controller and the second interface is a USB bus interface.

8. (original) A host controller as claimed in claim 1, wherein the internal memory is adapted to store multiple micro-frames of transfer descriptors, and to execute the stored transfer descriptors without intervention from the host microprocessor.

9. (original) A host controller as claimed in claim 8, wherein each of the multiple micro-frames of transfer descriptors may store payload data relating to one or more of isochronous, interrupt and bulk data transfers.

10. (original) A bus communication device, comprising:

a host microprocessor;

a system memory;

a memory bus, which connects the host microprocessor and the system memory; and

a host controller, wherein the host microprocessor is adapted to form transfer-based transfer descriptors, and write the transfer-based transfer descriptors to the system memory and to the host controller, and wherein the host controller comprises:

a first interface for connection to the memory bus, such that the host controller is adapted to act only as a slave on the memory bus;

an internal memory, for storing a plurality of transfer-based transfer descriptors received through the first interface; and

a second interface, for connection to an external bus,

wherein the host controller is adapted to:

execute stored transfer-based transfer descriptors;

update the content of the stored transfer-based transfer descriptors on execution; and

copy the updated stored transfer-based transfer descriptors to the system memory.

11. (original) A bus communication device as claimed in claim 10, wherein the second interface of the host controller is a USB bus interface, and the bus communication device is adapted to act as a USB host.

12. (original) A bus communication device as claimed in claim 10, wherein the host microprocessor is adapted to write a plurality of micro-frames of transfer descriptors to the system memory and to the host controller, and the host controller is adapted to execute the plurality of micro-frames of transfer descriptors without intervention from the host microprocessor.